HIGH-Q RF INDUCTORS ON STANDARD SILICON REALIZED USING WAFER-LEVEL PACKAGING TECHNIQUES

G. Carchon, S. Jenei, L. Carbonell, M. Van Hove, S. Decoutere, W. De Raedt, K. Maex, E. Beyne

IMEC, div. MCP-MaRS, Kapeldreef 75, B-3001 Heverlee, Belgium
E-mail: geert.carchon@imec.be; Tel: ++32/(0)16/288191; Fax: ++32/(0)16/281501

Abstract — **Wafer level packaging (WLP) techniques have been used to integrate state of the art high Q on-chip inductors on top of a five-levels-of-metal (5LM) Cu damascene back-end of line (BEOL) silicon process using 20 Ω.cm Si wafers. The inductors are realized above passivation using thick post-processed low-K dielectric (BCB) and Cu layers. For a BCB/Cu-thickness of 16 μm/10 μm, a peak Q-factor of 34 at 4.3 GHz has been obtained for a 1 nH inductor (substrate contacts present at both ports) with a resonance frequency of 29 GHz; the Q-factor further tops 30 over the 2.1-5.4 GHz frequency range. If a substrate contact is present at only 1 port, Q_{max} increases to 38 at 4.7 GHz. Patterned polysilicon ground shields further improve this performance: a Q-factor increase of 90% is demonstrated at 7 GHz for a 2.25 nH inductor. A good agreement between measurements and 3-D simulations is demonstrated.**

I. INTRODUCTION

Inductors integrated in today's typical silicon processes cannot meet the high performance specifications required for future RF ICs as they typically use an Al/Cu metallization to pattern the spiral and underpass [1, 2]. This metal is fairly resistive and, as the integration level increases, the metal thickness is typically thinned to decrease the achievable line pitch. This thinning of metal layers and their associated inter-layer dielectrics as process technologies advance, creates a fundamental problem for realizing high Q inductors on-chip. Increasing the inductor performance may be done by replacing the conventional Al/SiO_2 technology with low-K materials and thick Cu metallization [3], however, thick Cu is not a standard BEOL process and the dielectric in-between the spiral and the lossy silicon substrate, is still relatively thin.

A more attractive solution is to realize the inductors above passivation using post-processing techniques. In [4], 4 μm electroplated Cu and 9μm polyimide is used, resulting in a Q_{max} of 17. In [5, 6], Cu and BCB (benzocyclobutene, ε_r=2.65) are used to fabricate inductors with Q-factors as high as 26 on a 20 Ω.cm Si wafer, however, a floating substrate without BEOL was used. In this work, Q-factors up to 38 are demonstrated on top of a 5LM Cu damascene BEOL. The influence of substrate contacts and patterned ground shields is discussed and a comparison between measurements and 3-D simulations is performed.

II. TECHNOLOGY DESCRIPTION

Thin-film technology offers the advantage of high precision, low temperature and low cost. In this way, it has been used successfully in the past for the realization of high-Q passives off-chip and SiP based RF circuits [7].

A cross section of the post-processing concept is shown in Fig. 1: thin-film layers are processed above passivation. The post-processed metals can at the same time be used to realize low loss interconnects [6] or flip-chip redistribution, hereby making the process compatible with WLP. As metal layers are added above passivation, one may reduce the number of BEOL-metals, hereby reducing costs. The process is also compatible with an Al and a Cu BEOL.

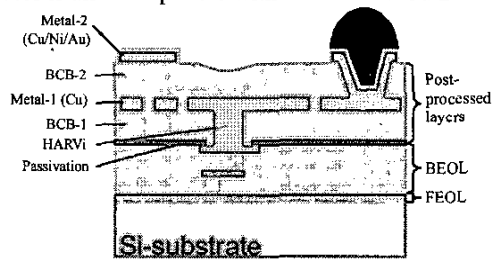

Fig. 1: Schematic cross section of the "inductor above passivation"-concept: thick thin-film layers are post-processed on top of the passivation. An Al as well as Cu BEOL may be used.

The inductors realized in this work have been fabricated on top of a 5LM Cu damascene BEOL process using 20Ω.cm Silicon wafers. The back-end Cu-layers and inter-metal dielectrics (oxide) have a thickness of respectively 625 nm and 475 nm, hereby creating a standoff of about 6 μm between the SiN passivation and the substrate. The post-processed inductors have been realized on top of the passivation using two different process flows. The realized thicknesses are summarized in Table 1.

In flow-1, a photo-BCB (BCB-1) is deposited first. In this layer, the electrical contacts to the underlying BEOL are opened. Metal-1 then directly makes a connection to the top BEOL layer. As the aspect ratio of standard photo-BCB via connections is <1:4, relatively large vias are needed when the BCB-thickness is increased above 5 μm.

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Table 1: BCB and Cu thicknesses realized in flow-1 and flow-2. The location of the different layers is explained in Fig. 1.

	BCB-1	Metal-1	BCB-2	Metal-1 pitch
flow-1	5 μm	5 μm	8 μm	10 μm
flow-2	16 μm	10 μm	12 μm	20 μm

To keep the size and pad capacitance of the via small when the BCB-thickness is increased, a special high aspect ratio via structure (HARVi) has been used in flow-2: first, a metal stud is plated on top of the BEOL layers, then BCB-1 is deposited. Due to planarization, only a thin layer of BCB is present on top of the HARVi. This thin layer is opened using conventional photolithography. The method results in high yield via connections with diameters as small as 10 μm in a 20 μm thick BCB layer. A FIB cross section of a flow-2 stack is shown in Fig. 2.

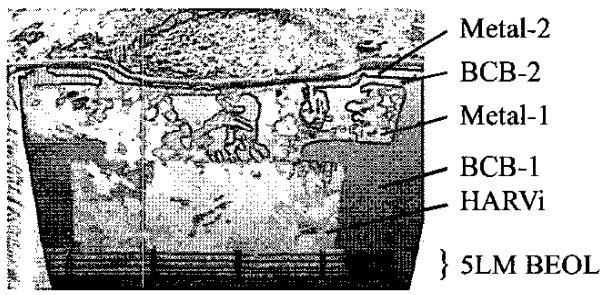

Fig. 2: FIB cross section of a flow-2 stack showing 5 BEOL metals, HARVi, 10 μm thick electroplated Cu and overpass.

The layout parameters of the inductors, discussed in this work, are given in Table 2 (meaning illustrated in Fig. 3).

To connect the inner part of the inductor with the outer part, an underpass in the BEOL layers or a post-processed overpass (metal-2) can be used as shown in Fig. 3 and Fig. 4. Unless otherwise stated, the inductors described in this work contain substrate contacts located underneath the ground pads and an overpass on Metal-2 is always used in combination with an underpass on the 5th BEOL metal.

Table 2: Inductor layout parameters (meaning shown in Fig. 3).

Inductor	N	W (μm)	S (μm)	Din (μm)	Dout (μm)	Area (mm^2)	Shield Present
L1	2.5	10	10	110	50	0.035	No
L2	3.5	10	10	110	50	0.049	No
L3	1.5	20	10	215	50	0.078	No
L4	2.5	20	10	215	50	0.110	No
L5	2.5	20	10	215	50	0.110	Yes
L6	4.5	20	10	215	50	0.192	No

III. Measured Performance

Measurements have been performed using Picoprobes and an HP8510 network analyzer. After an initial SOLT calibration on the calibration substrate, the pad parasitics are removed by measuring an on-wafer short and open. The resulting reference plane location is shown in Fig. 3. The probe contact resistance was in the mΩ range.

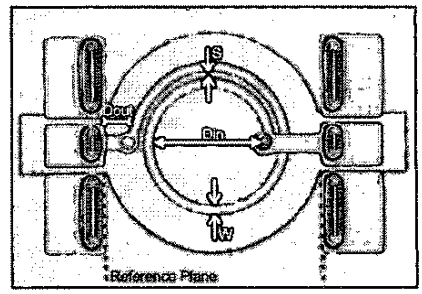

Fig. 3: Inductor L3 (flow-2): an overpass on metal-2 is used in combination with an underpass on the 5th BEOL metal layer.

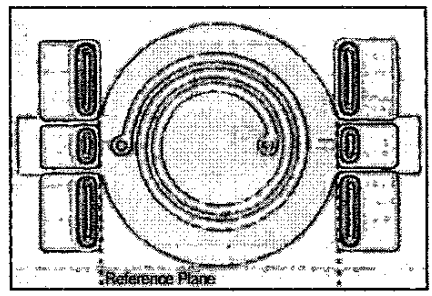

Fig. 4: Inductor L5 (split-2): an underpass on the 5th BEOL metal layer is used. A patterned polysilicon ground shield is present below the inductor.

The inductor's Q-factor has been determined from the measurements using the relation

$$Q = imag(1/Y_{11})/real(1/Y_{11}) \quad (1)$$

The measured performance of inductor L3, realized in flow-1 and flow-2, is shown in Fig. 5. The layouts use an overpass on metal-2 in parallel with an underpass on the 5th BEOL metal layer. In this way, the measurements take the increase in parasitic capacitance into account, present when the inductor is connected to the BEOL.

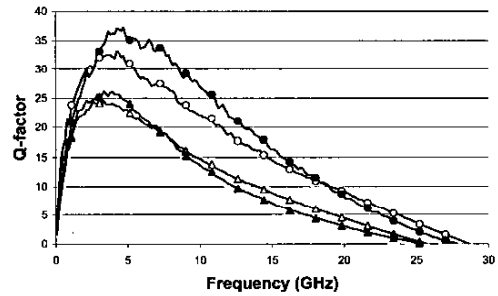

Fig. 5: Measured Q-factor for inductor L3: substrate contacts at both ports in flow-1 (-Δ-), flow-2 (-o-); substrate contact at 1 port in flow-1 (-▲-), flow-2 (-●-).

Using the 5 μm thick Cu layer (flow-1), a maximum Q-factor of 24@2.6GHz has been obtained; Q_{max} increases to

34@4.2GHz for the 10 μm thick Cu realization (flow-2) while the Q-factor tops 30 over the 2.1-5.4 GHz frequency band. If a substrate contact is only present at 1 port, Q_{max} increases further to 26 (flow-1) and 38 (flow-2).

The measured performance of the other inductors (substrate contacts at both ports) is summarized in Table 3. It may be observed that Q_{max} in flow-2 is about 35% higher than those obtained in flow-1.

Table 3: Measured inductor performance for flow-1 and flow-2, an underpass has been used in parallel with an overpass, substrate contacts are present at both ports.

	Flow-1				Flow-2			
	L_s (nH)	Q_{max}	F_{Qmax} (GHz)	F_{res} (GHz)	L_s (nH)	Q_{max}	F_{Qmax} (GHz)	F_{res} (GHz)
L1	1.17	18.7	4.4	27	1.13	25	4.4	30
L2	2.28	16.2	2.6	16	2.18	22	2.9	18.5
L3	0.97	24.5	3.3	25.8	0.93	34	4.2	28.5
L4	2.35	20.6	1.5	13	2.25	28	2.1	15
L5	2.22	23.7	3.3	9	2.18	31.4	4.4	12
L6	7.11	16.9	0.8	5	6.9	23	1.2	6.5

IV. Influence of a Patterned Grounded Polysilicon Shield

As for BEOL-inductors [8], patterned ground shields may be used to decrease the substrate induced losses, hereby increasing the performance of the post-processed on-chip inductors. In this work, a patterned polysilicon ground shield has been used (cf. Fig. 4). The obtained performance is shown in Fig. 6: the use of the shield increases Q_{max} by about 10%, however, the effect is more pronounced at higher frequencies, e.g., at 7 GHz the Q-factor increases by as much as 90% for the realization in flow-2. The reduction in resonance frequency is relatively small.

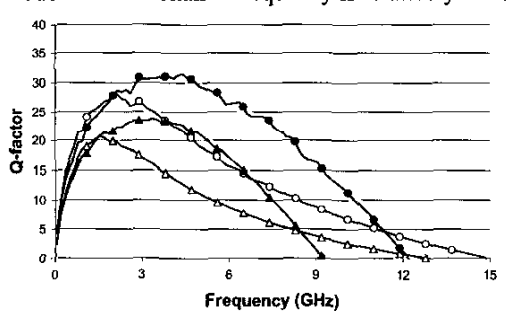

Fig. 6: Measured Q-factor for inductor L4: (-Δ-) flow-1 and (-o-) flow-2 without shield, (-▲-) flow-1 and (-●-) flow-2 with shield.

In Fig. 7, the extracted inductance ($Ls=-imag(1/Y_{21})/\omega$) is given for inductor L4, with and without patterned polysilicon ground shield. It may be noticed that the presence of the shield only has a limited influence on the extracted series inductance. The latter is especially true for flow-2.

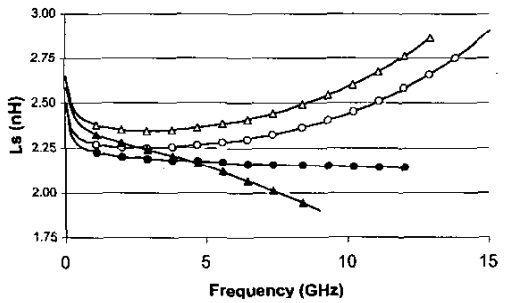

Fig. 7: Extracted inductance as a function of frequency for inductor L4: (-Δ-) flow-1 and (-o-) flow-2 without shield, (-▲-) flow-1 and (-●-) flow-2 with shield.

V. Influence of Substrate Contacts

Substrate contacts only had a limited influence on the inductor's performance: a floating substrate resulted in a slightly higher Q_{max}, mainly due to slightly lower parasitic capacitances to ground. The measured Q-factors for inductor L4 (flow-1 and flow-2) with and without substrate contacts are shown in Fig. 8, the S-parameters are shown in Fig. 9.

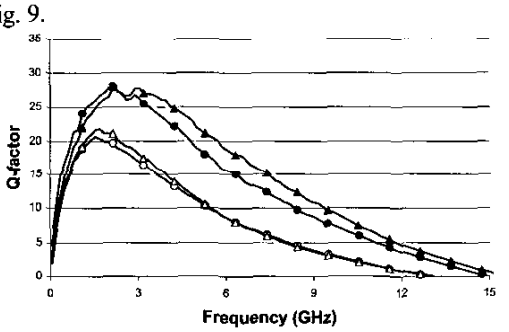

Fig. 8: Measured Q-factor for inductor L4: flow-1 without (-Δ-) and with substrate contacts (-o-), flow-2 without (-▲-) and with substrate contacts (-●-).

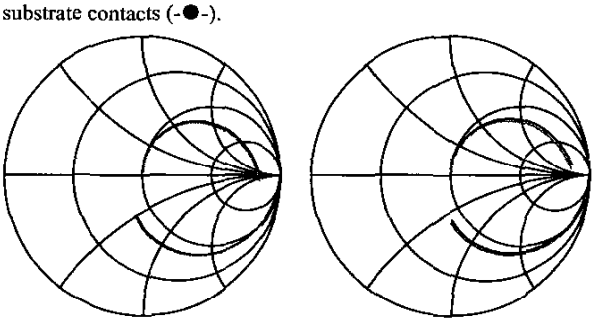

Fig. 9: S_{11} and S_{21} of inductor L4 realized in flow-1 (left) and flow-2 (right) with (grey) and without (black) substrate contacts at the inputs.

VI. UNDERPASS VERSUS UNDERPASS//OVERPASS

The inner part of the spiral may be connected to, the outer part using a metal-2 overpass, a BEOL underpass, or a combination. The obtained performance for inductor L3 (flow-1) is shown in Fig. 10: the use of a 20 μm wide underpass on the 5th BEOL metal reduces Q_{max} from 24.5 to 19, no effect on resonance frequency is observed as the underpass (and associated parasitic capacitance) is included in both realizations. The performance of the underpass realization could be increased by shunting several BEOL layers or by increasing the width of the underpass. A pure overpass realization would also increase the performance.

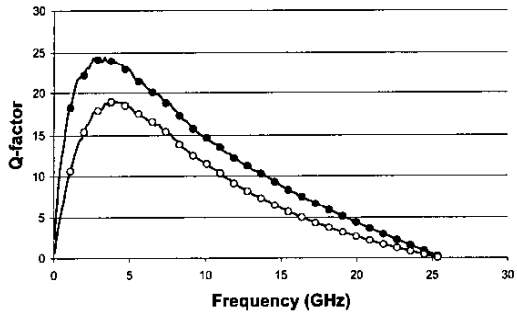

Fig. 10: Measured Q-factor for inductor L3 (flow-1) using a 20μm wide underpass on the 5th BEOL-metal (-o-), or using a 30μm wide overpass in parallel with the BEOL underpass (-●-).

VII. 3-D SIMULATIONS

The post-processed inductors have been simulated using Ansoft HFSS. A good agreement between the measured (floating substrate) and simulated performance has been obtained as may be observed in Fig. 11 and Fig. 12: for the lower frequency range, the fields were solved inside the metals, for the higher frequencies, a solve surface approach proved to be sufficient. The overall result uses the lowest value obtained in both simulations.

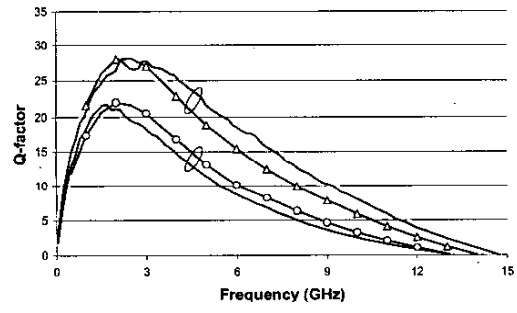

Fig. 11: Measured (-) versus simulated Q-factor for inductor L4 in flow-1 (-o-) and flow-2 (-Δ-).

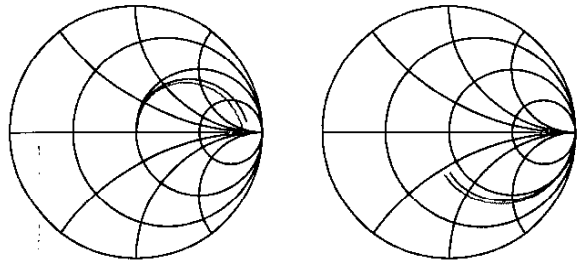

Fig. 12: Measured (grey) versus simulated (black) S_{11} (left) and S_{21} (right) for inductor L4, realized in split-2 (floating substrate).

VIII. CONCLUSIONS

WLP-techniques have been used to integrate high Q on-chip inductors on top of a five-levels-of-metal Cu damascene back-end of line (BEOL) silicon process using 20Ωcm Si wafers. The inductors are realized above the passivation using thick post-processed BCB and Cu. For a BCB/Cu-thickness of 16μm/10μm, a peak Q-factor of 34 at 4.3 GHz has been obtained for a 1 nH inductor. If a substrate contact is present at only 1 port, Q_{max} increases to 38 at 4.7 GHz. Patterned polysilicon ground shields may significantly improve the performance: a Q-factor increase of 90% was demonstrated at 7 GHz for a 2.25 nH inductor. The influence of substrate contacts has been investigated as well as the trade-off between a post-processed overpass or a BEOL underpass. A good agreement between measurements and 3-D simulations was demonstrated.

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